REMARKS

Claims remaining in the present patent application are Claims 1-10 and 21-30. The Applicant respectfully requests consideration of the above captioned patent application in light of the remarks presented herein.

35 U.S.C. § 103(a) Rejections

Claims 1-10 and 21-30 stand rejected under 35 USC § 103(a) as being allegedly unpatenable over Chidambarrao et al. (US 6,707,095, "Chidambarrao") in view of Blanchard (US 6,576,516, "Blanchard"). Applicant has reviewed the cited references and respectfully asserts that embodiments in accordance with the present invention as recited in Claims 1-10 and 21-30 are not rendered obvious over Chidambarrao in view of Blanchard.

Applicant respectfully traverses the rejection's proposed motivation to modify Chidambarrao in view of Blanchard to "result in substantially reduced on-resistance" to realize embodiments of the present invention as recited in Claims 1-10 and 21-30. Blanchard is relied upon primarily to teach a polysilicon fill. Blanchard does not achieve reduced on-resistance due to a polysilicon fill, but rather due to "alternating columns of opposite doping type" (column 2, lines 19-20). Thus, Applicant respectfully asserts that Chidambarrao in view of Blanchard does not teach or suggest the suggested benefit proposed by the rejection.

For this reason, Applicant respectfully asserts that all rejections based upon a combination of Chidambarrao in view of Blanchard are overcome, and respectfully solicits allowance of claims 1-10 and 21-30.

Assuming, *arguendo*, that Blanchard's polysilicon fill would reduce the on-resistance of Chidambarrao's memory cell structure, there is no motivation in the cited combination for such a modification. Applicant does not find a suggestion or motivation in Chidambarrao or Blanchard that Chidambarrao's memory cell structure would benefit from a reduced on-resistance.

For this additional reason, Applicant respectfully asserts that all rejections based upon a combination of Chidambarrao in view of Blanchard are overcome, and respectfully solicits allowance of claims 1-10 and 21-30.

Further, according to Blanchard Figure 2, an improvement in on-resistance is not apparent until a breakdown voltage of about 150 volts. Applicant respectfully asserts that such a high voltage effect would have no impact on Chidambarrao's memory cells that are intended to operate at substantially much lower voltages, e.g., "a '1' (1.5V) level" (column 8, lines 9-10).

For this further reason, Applicant respectfully asserts that all rejections based upon a combination of Chidambarrao in view of Blanchard are overcome, and respectfully solicits allowance of claims 1-10 and 21-30.

Applicant respectfully asserts that the combination of Chidambarrao and Blanchard does not teach or suggest the claimed embodiments of the present invention. Chidambarrao is directed to dense, low voltage memory cells whereas Blanchard is directed to high voltage power MOSFETs. Applicant respectfully asserts that one of ordinary skill in the art would not be motivated to combine these two references in order to produce embodiments in accordance with the present claimed invention.

For this still additional reason, Applicant respectfully asserts that all rejections based upon a combination of Chidambarrao in view of Blanchard are overcome, and respectfully solicits allowance of claims 1-10 and 21-30.

With respect to Claims 1-10 and 21-30, Applicant respectfully asserts that Chidambarrao in view of Blanchard does not teach or suggest the limitation of "a polysilicon fill disposed on the surface of said silicon dioxide layer and on a portion of said wall" as recited by Claims 1-10 and 21-30. In contrast, Chidambarrao teaches a silica, SiO_2, filling of a trench (Figure 9C, SiO_2 26). By teaching filling a trench with silica, Chidambarrao actually teaches away from embodiments in accordance with the present invention as recited in Claims 1-10 and 21-30 that recite a polysilicon fill.

For this additional reason, Applicant respectfully asserts that Claims 1-10 and 21-30 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Further with respect to Claim 1, Applicant respectfully asserts that Chidambarrao in view of Blanchard does not teach or suggest the limitation of "a silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated at a distance D below said planar surface of said silicon device" as recited by Claim 1. Applicant respectfully asserts that Chidambarrao is silent with respect to terminating a layer of silicon dioxide below the planar surface of a silicon device. However, the Figures of Chidambarrao, for example Figure 9C, *inter alia*, appear to indicate that a layer of silicon dioxide is continuous all the way up to the silicon surface, in contrast to the embodiments of the instant claim.

Blanchard does not correct this deficiency, as Blanchard does not teach a silicon dioxide trench lining.

For this additional reason, Applicant respectfully asserts that Claim 1 overcomes the rejections of record, and respectfully solicits allowance of this Claim.

Claims 2-10 depend from Claim 1. Applicant respectfully asserts that these claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicits allowance of these Claims.

Further with respect to Claim 3, Applicant respectfully asserts that Chidambarrao in view of Blanchard does not teach or suggest the limitation of "electronic silicon device ... comprising a junction field effect transistor (JFET)" as recited by Claim 3. Applicant respectfully asserts that Chidambarrao is silent with respect to constructing a JFET from a trench structure. The trench structures of Chidambarrao are consistently described as either metal oxide semiconductor field effect transistors (MOSFETs), capacitors or isolation structures. Applicant respectfully asserts that one of ordinary skill in the art would understand a significant difference between the recited JFET and Chidambarrao's MOSFETs.

Blanchard does not correct this deficiency, as Blanchard teaches a "high voltage power MOSFET" and does not teach JFETs.

For this additional reason, Applicant respectfully asserts that Claim 3 overcomes the rejections of record, and respectfully solicits allowance of this Claim.

With respect to Claim 21, Applicant respectfully asserts that Chidambarrao in view of Blanchard does not teach or suggest the limitation of "a

silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated below an original surface of said silicon substrate" as recited by Claim 21, for the rationale presented previously with respect to Claim 1.

For this additional reason, Applicant respectfully asserts that Claim 21 overcomes the rejections of record, and respectfully solicits allowance of this Claim.

Claims 22-30 depend from Claim 21. Applicant respectfully asserts that these claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicits allowance of these Claims.

Further with respect to Claim 23, Applicant respectfully asserts that this claim overcomes the rejections of record for the same rationale presented previously with respect to Claim 3. For this additional reason, Applicant respectfully asserts that Claim 23 overcomes the rejections of record, and respectfully solicits allowance of this Claim.

CONCLUSION

Claims remaining in the present patent application are Claims 1-10 and 21-30.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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